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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,956	UKON ET AL.	
	Examiner	Art Unit	
	SALVADOR E. RIVAS	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is in response to Applicant's arguments filed on November 25, 2008. **Claims 1-7 and 9-20** are now pending in the present application. **This Action is made Final**.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-5, 7-11, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rolston et al. (U.S. Patent Application Publication #2002/0031199 A1)** in view of **Cedrone et al. (US Patent # 6,538,987 B1)**.

Regarding **claims 1 and 16**, Rolston et al. teach a synchronous clock supply system ("a method and apparatus for synchronizing clocking at distributed nodes in synchronized electronic, optical or optoelectronic systems, such as computing or switching systems." Paragraph [0010]) comprising:

at least one relay node (Fig.1 @ N1) which is positioned in a clock supply route formed by coupling arbitrary virtual paths for a loop of nodes in a network (Fig.1 @ 10, "... a method of providing synchronized clock signals at "In" distributed nodes in a synchronous system, the nodes comprising a master node and a plurality of slave nodes interconnected by first and second propagation channels." Paragraph ([0011])); and

a termination node (Fig.2 @ N2, N3, N4, N5, N6, N7, N8) which is positioned in a downstream side of the clock supply route farther than the relay node from a synchronous clock sending source (read as Master Node (Fig.2 @ N1)) used to synchronize the nodes in the network, and finally receives the synchronous clock via a predetermined port (Fig.2).

However Rolston fails to teach the relay node having

fault detection means for, when no synchronous clock is supplied in a

downstream direction from an upstream side of the clock supply route due to a fault in the virtual path, detecting that no synchronous clock is supplied,

fault notification data transmission means for, when said fault detection means detects the fault,

sending fault notification data representing occurrence of the fault to the downstream side of the clock supply route, and

first port switching means for, when switching instruction data designating switching to another port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route,

switching a port for receiving the synchronous clock to the port, and

the termination node having second port switching means for, when another port is connected to the sending source via another virtual path and the fault notification data is sent from the relay node,

performing port switching for supplying the synchronous clock from the predetermined port to said another port,

the first and second port switching means forming upstream and downstream switching ports, and

port switching instruction means for, when said port switching means performs port switching,

sending switching instruction data which instructs the upstream side of the clock supply route to switch the port to said another port for supply of the synchronous clock.

Cedrone et al. teach a system for "... employing the inventive rapid ring

protection switching sets up corresponding virtual circuits over both the selected ring and the non-selected ring." (Column 3 Lines 36-38) Furthermore, Cedrone et al. teach a relay node having

fault detection means for, when no synchronous clock is supplied in a downstream direction from an upstream side of the clock supply route due to a fault in the virtual path, detecting that no synchronous clock is supplied ("The system also uses a novel detection mechanism for detecting, without significant delay, the path failures and path degradation that trigger protection switching events." Column 6 Lines 23-26),

fault notification data transmission means for, when said fault detection means detects the fault, sending fault notification data representing occurrence of the fault to the downstream side of the clock supply route ("To detect an event that triggers protection switching, such as path failure, the system 10 uses "Continuity OAM cells" to provide path status information to the nodes." Column 4 Lines 24-26), and

first port switching means for (read as node processor (Fig.3 @ 42)), when switching instruction data designating switching to another port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route ("Each destination node determines if it should initiate protection switching based on the number of Continuity OAM cells received from the source node over both the selected and the non-selected routes." Column 8 Lines 42-46),

switching a port for receiving the synchronous clock to the port ("Each node 12 receives information over the rings 14 and 16 through incoming ports 20 and sends information over the rings through destination ports 22." Column 5 Lines 44-46), and

the termination node (read as destination node (Fig.1 @ 12)) having second port switching means for, when another port is connected to the sending source via another virtual path and the fault notification data is sent from the relay node ("Each node 12 receives information over the rings 14 and 16 through incoming ports 20 and sends information over the rings through destination ports 22." Column 5 Lines 44-46),

performing port switching for supplying the synchronous clock from the predetermined port to said another port ("Each destination node determines if it should initiate protection switching based on the number of Continuity OAM cells received from the source node over both the selected and the non-selected routes." Column 8 Lines 42-46),

the first and second port switching means forming upstream and downstream switching ports ("Each node 12 receives information over the rings 14 and 16 through incoming ports 20 and sends information over the rings through destination ports 22." Column 5 Lines 44-46), and

port switching instruction means for, when said port switching means performs port switching ("When a segment of the selected route, in the example, the primary ring 14, fails or becomes sufficiently degraded, an affected destination node 12 initiates a protection switch. The destination node thus selects the secondary ring 16 as the route for the affected virtual paths." (Column 7 Lines 33-37) Furthermore, enabling the routing information "... in the secondary set of tables 36 ... for all of the virtual circuits in the affected virtual paths, while the corresponding routing information is simultaneously disabled in the primary set of tables 30, and the protection switching is complete."

(Column 7 Lines 45-50)),

sending switching instruction data which instructs the upstream side of the clock supply route to switch the port to said another port for supply of the synchronous clock. (read as the node (Fig.1 @ 12, Fig.3) multicasts the "Continuity OAM cell" "…. to its local node processor 42 for processing, and, without alteration, along the same ring to successive nodes 12. The Continuity OAM cells thus travel around the system 10 in both directions at predetermined intervals." Column 8 Lines 33-37)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the path degradation/failure detection mechanism and ring protection mechanism as taught by Cedrone et al. within the apparatus to provide synchronous clocking as taught by Rolston et al. for the purpose of employing rapid ring protection switching within ring architecture that provides synchronous clocking.

Regarding **claim 7**, Rolston et al. teach a synchronous clock supply method ("a method and apparatus for synchronizing clocking at distributed nodes in synchronized electronic, optical or optoelectronic systems, such as computing or switching systems." Paragraph [0010]) comprising the steps of:

sending a synchronous clock used to synchronize nodes in a network from a synchronous clock sending source to a termination node along a predetermined clock supply route via a plurality of nodes (Fig.1 @ 10, "… a method of providing synchronized clock signals at "In" distributed nodes in a synchronous system, the nodes

comprising a master node and a plurality of slave nodes interconnected by first and second propagation channels." Paragraph ([0011]));

However, Rolston et al. fails to teach when the synchronous clock sent in the synchronous clock sending step generates a fault in a line after the synchronous clock sending source,

detecting the fault at a predetermined port at a nearest downstream node in the fault generated line;

sending fault notification data representing occurrence of the fault from the detecting node in the fault detection step to the termination node;

when the fault notification data sent in the fault notification data sending step reaches the termination node,

switching a port for receiving the synchronous clock to a port which is connected to a path other than the synchronous clock sending source and the clock supply route and is different from the port that has received the fault notification data at the termination node, and

sending back switching instruction data representing port switching by coupling arbitrary virtual paths for nodes; and

switching the receiving port to a synchronous clock reception port at each node which has received the switching instruction data sent in the port switching instruction step.

Cedrone et al. teach a system for "... employing the inventive rapid ring protection switching sets up corresponding virtual circuits over both the selected ring

and the non-selected ring." (Column 3 Lines 36-38) Furthermore, Cedrone et al. teach a method for when the synchronous clock sent in the synchronous clock sending step generates a fault in a line after the synchronous clock sending source ("The system also uses a novel detection mechanism for detecting, without significant delay, the path failures and path degradation that trigger protection switching events." Column 6 Lines 23-26),

sending fault notification data representing occurrence of the fault from the detecting node in the fault detection step to the termination node ("To detect an event that triggers protection switching, such as path failure, the system 10 uses "Continuity OAM cells" to provide path status information to the nodes." Column 4 Lines 24-26);

when the fault notification data sent in the fault notification data sending step reaches the termination node ("Each destination node determines if it should initiate protection switching based on the number of Continuity OAM cells received from the source node over both the selected and the non-selected routes." Column 8 Lines 42-46),

switching a port for receiving the synchronous clock to a port which is connected to a path other than the synchronous clock sending source and the clock supply route and is different from the port that has received the fault notification data at the termination node (Fig.3, "When a segment of the selected route, in the example, the primary ring 14, fails or becomes sufficiently degraded, an affected destination node 12 initiates a protection switch. The destination node thus selects the secondary ring 16 as the route for the affected virtual paths." (Column 7 Lines 33-37) Furthermore, enabling

the routing information "... in the secondary set of tables 36 ... for all of the virtual circuits in the affected virtual paths, while the corresponding routing information is simultaneously disabled in the primary set of tables 30, and the protection switching is complete." (Column 7 Lines 45-50)), and

first port switching means for (read as node processor (Fig.3 @ 42)), when switching instruction data designating switching to another port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route ("Each destination node determines if it should initiate protection switching based on the number of Continuity OAM cells received from the source node over both the selected and the non-selected routes." Column 8 Lines 42-46),

sending back switching instruction data representing port switching by coupling arbitrary virtual paths for nodes ((Fig.1 @ 12, Fig.3), "Each node 12 receives information over the rings 14 and 16 through incoming ports 20 and sends information over the rings through destination ports 22." Column 5 Lines 44-46); and

switching the receiving port to a synchronous clock reception port at each node which has received the switching instruction data sent in the port switching instruction step (read as the node (Fig.1 @ 12, Fig.3) multicasts the "Continuity OAM cell" "…. to its local node processor 42 for processing, and, without alteration, along the same ring to successive nodes 12. The Continuity OAM cells thus travel around the system 10 in both directions at predetermined intervals." Column 8 Lines 33-37).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the path degradation/failure detection

mechanism and ring protection mechanism as taught by Cedrone et al. within the apparatus to provide synchronous clocking as taught by Rolston et al. for the purpose of employing rapid ring protection switching within ring architecture that provides synchronous clocking.

Regarding **claims 2 and 17**, and **as applied to claims 1 and 16 above**, Rolston et al, as modified by Cedrone et al., teach a system (Fig. 2 @ 10) further comprising clock sending means for sending the synchronous clock to the clock supply route (Paragraph [0044]).

Regarding **claims 3 and 18**, and **as applied to claims 1 and 16 above**, Rolston et al, as modified by Cedrone et al., teach a system (Fig. 2 @ 10) wherein the clock supply route includes a plurality of clock supply routes (Paragraph [0041], Lines 1-2),

the synchronous clock is sent to the respective clock supply routes (Paragraph [0041], Lines 5-8),

the relay node includes relay nodes for the respective clock supply routes (Paragraph [0039], Lines 1-3), and

the termination node includes termination nodes for the respective clock supply routes. (Paragraph [0039], Lines 11-14)

Regarding **claims 4 and 9**, and **as applied to claims 1 and 7 above**, Rolston et al. teach a method and apparatus for "… synchronizing clocking at distributed nodes in synchronized electronic, optical or optoelectronic systems, such as computing or switching systems." (Paragraph [0010])

wherein the synchronous clock includes a synchronous clock which is obtained by extracting a frequency component from a signal used for communication between the nodes ("The step of maintaining the pulse rate may comprise the step of dividing the frequency of the first and second pulse trains by an integer multiple of the number of nodes ..." Paragraph [0022] Lines 1-4) and

has a unit time as a period. ("... the master node unit comprising: pulse generation means for providing a first pulse train and a second pulse train, the pulse trains each being regular and both having the same period;" Paragraph [0023] Lines 6-9)

However, Rolston fails to teach said fault notification data transmission means sends the fault notification data as part of an ATM cell,

when the switching instruction data is sent as part of an ATM cell from the upstream direction,

said first port switching means switches the port for receiving the synchronous clock to a port which receives the switching instruction data,

when the fault notification data is sent as part of the ATM cell from the relay node, said second port switching means switches the port for supplying the synchronous clock from the predetermined port to said another port, and

said port switching instruction means sends the switching instruction data as part of an ATM cell.

Cedrone et al. teach a system (Fig.1 @ 10) for "... employing the inventive rapid ring protection switching sets up corresponding virtual circuits over both the selected

ring and the non-selected ring." (Column 3 Lines 36-38) Furthermore, Cedrone et al. teach fault notification data transmission means (read as node (Fig.1 @ 12, Fig.3) with node processor (Fig.3 @ 42)) sends the fault notification data (read as system (Fig1 @ 10) uses "Continuity OAM cells" to provide path status information to the nodes." Column 4 Lines 24-26)) as part of an ATM cell ("... system 10 may, for example, be a unidirectional SONET ring, with information in the form of ATM cells and frames transmitted in both directions over the primary and secondary rings." Column 5 Lines 40-43),

when the switching instruction data is sent as part of an ATM cell from the upstream direction ("... system 10 may, for example, be a unidirectional SONET ring, with information in the form of ATM cells and frames transmitted in both directions over the primary and secondary rings." Column 5 Lines 40-43),

said first port switching means (read as node processor (Fig.3 @ 42)) switches the port for receiving the synchronous clock to a port which receives the switching instruction data ("Each destination node determines if it should initiate protection switching based on the number of Continuity OAM cells received from the source node over both the selected and the non-selected routes." Column 8 Lines 42-46),

when the fault notification data (read as Continuity OAM cell) is sent as part of the ATM cell from the relay node, said second port switching means switches the port for supplying the synchronous clock from the predetermined port to said another port (Fig.3) ("When a segment of the selected route, in the example, the primary ring 14, fails or becomes sufficiently degraded, an affected destination node 12 initiates a

protection switch. The destination node thus selects the secondary ring 16 as the route for the affected virtual paths." (Column 7 Lines 33-37) Furthermore, enabling the routing information "… in the secondary set of tables 36 … for all of the virtual circuits in the affected virtual paths, while the corresponding routing information is simultaneously disabled in the primary set of tables 30, and the protection switching is complete." (Column 7 Lines 45-50)), and

said port switching instruction means sends the switching instruction data as part of an ATM cell ((read as the node (Fig.1 @ 12, Fig.3) multicasts the "Continuity OAM cell" "…. to its local node processor 42 for processing, and, without alteration, along the same ring to successive nodes 12. The Continuity OAM cells thus travel around the system 10 in both directions at predetermined intervals." (Column 8 Lines 33-37) Furthermore, system (Fig.1 @10) "… for example, be a unidirectional SONET ring, with information in the form of ATM cells and frames transmitted in both directions over the primary and secondary rings." Column 5 Lines 40-43).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the path degradation/failure status alert mechanism and ring protection mechanism as taught by Cedrone et al. within the apparatus to provide synchronous clocking as taught by Rolston et al. for the purpose of employing rapid ring protection switching within ring architecture that provides synchronous clocking.

Regarding **claim 5**, and **as applied to claim 4 above**, Rolston et al., as modified by Cedrone et al., teach a system (Fig.2 @ 10) wherein the clock supply route includes a plurality of clock supply routes (Paragraph [0041], Lines 1-2),

the synchronous clock is sent to the respective clock supply routes (Paragraph [0041], Lines 5-8),

the relay node includes relay nodes for the respective clock supply routes (Paragraph [0039], Lines 1-3), and

the termination node includes termination nodes for the respective clock supply routes. (Paragraph [0039], Lines 11-14)

Regarding **claims 10, 11, and 19**, and **as applied to claims 1, 7, and 16 above**, Rolston et al, as modified by Cedrone et al. teach a system (Fig.1 @ 10) wherein there are four nodes (Fig.1 @ N1, N2, N3 , N4).

Regarding **claim 14**, and **as applied to claim 7 above**, Rolston et al., as modified by Cedrone et al. teach a method wherein the plurality of nodes form a loop (Fig.1).

Regarding **claim 15**, and **as applied to claim 7 above**, Rolston et al., as modified by Cedrone et al. teach a method wherein the ports comprise upstream and downstream ports (Fig.1 @ 20, 22, Fig.2 @ 20, 22, Fig.3 @ 20, 22; Column 5 Lines 44-46).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Rolston et al. (U.S. Patent Application Publication #2002/0031199 A1)**, in view of **Cedrone et**

al. (US Patent # 6,538,987 B1), and further in view of **Puleston (U.S. Patent # 2002/0181480 A1)**.

Regarding **claim 6**, and **as applied to claim 1 above**, Rolston et al. teach a method and apparatus for "... synchronizing clocking at distributed nodes in synchronized electronic, optical or optoelectronic systems, such as computing or switching systems." (Paragraph [0010])

Cedrone et al. teach a system (Fig.1 @ 10) for "... employing the inventive rapid ring protection switching sets up corresponding virtual circuits over both the selected ring and the non-selected ring." (Column 3 Lines 36-38)

However, Rolston et al. and Cedrone et al. fail to teach wherein a priority is set for a port to be switched, and

a clock supply line priority table representing a priority for port switching for supplying the synchronous clock is prepared at each node.

Puleston teaches a method for "... storing a routing table having a plurality of routes associated with a plurality of networks, each being identified by a network address." (Paragraph [0013] Lines 1-3) Furthermore, Puleston teaches a method wherein a priority is set for a port to be switched, and a clock supply line priority table (read as routing table) representing a priority for port switching for supplying the synchronous clock is prepared at each node ("... a router stores a routing table which includes information on which connections lead to particular groups of addresses, priorities for connections to be used, and rules for handling both routine and special cases of traffic." Paragraph [0003] Lines 6-10).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the mechanism for identifying and executing priority connections based on data from a routing table as taught by Puleston with the path degradation/failure detection mechanism and ring protection mechanism as taught by Cedrone et al. within the apparatus to provide synchronous clocking as taught by Rolston et al. for the purpose of employing rapid ring protection switching within ring architecture that provides synchronous clocking.

Claim 12, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rolston et al. (U.S. Patent Application Publication #2002/0031199 A1)**, in view of **Cedrone et al. (US Patent # 6,538,987 B1),** and further in view of **Seki et al. (U.S. Patent Application Publication #2004/0213247 A1)**.

Regarding **claims 12, 13, and 20**, and **as applied to claims 1, 7, and 16 above**, Rolston et al. teach a method and apparatus for "… synchronizing clocking at distributed nodes in synchronized electronic, optical or optoelectronic systems, such as computing or switching systems." (Paragraph [0010]) Furthermore, Rolston et al. teach a system comprising of:

a control unit (Fig. 2 @ 62);

a line master unit connected to the control unit (Fig.2);

a linearly connected clock generation source (Fig.2 @ 18) and clock input circuit connected to the line master unit (Fig.2 @ POST1A, POST1B); and

Cedrone et al. teach a system (Fig.1 @ 10) for "… employing the inventive rapid ring protection switching sets up corresponding virtual circuits over both the selected

ring and the non-selected ring." (Column 3 Lines 36-38) Furthermore, Cedrone et al. teach a system comprising of:

a control unit (Fig. 2 @ 42);

a clock supply line priority table (read as routing tables (Fig.2 @ 32, 34, 38, 40)) connected to the control unit (read as node processor (Fig.2 @ 42));

However, Rolston et al. and Cedrone et al. fail to teach a system wherein at least one node is a switching unit comprising:

a linearly arranged input line unit ATM switch and output line unit, each connected to the control unit;

at least one clock input circuit connected to the line master unit.

Seki et al. teach a communication network system and method (read as ATM node (Fig.7)) for "... synchronously controlling path connection for instantaneously controlling path connection at a predesignated time." (Paragraph [0002]) Furthermore, Seki et al. teach a system (Fig.7 @ 20) wherein at least one node is a switching unit comprising:

a control unit (Fig.7 @ 40);

a linearly arranged input line unit (Fig.7 @ 50-1 - 50-m) ATM switch (Fig.7 @ 80) and output line unit (Fig.7 @ 70-1 - 70-m), each connected to the control unit (Fig.7 @ 40); and

at least one clock input circuit (Fig.7 @ 50-1 - 50-m) connected to the line master unit (Fig.7 @ 41) (Paragraph [0068]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the switching mechanism as taught by Seki et al. with the path degradation/failure detection mechanism and ring protection mechanism as taught by Cedrone et al. within the apparatus to provide synchronous clocking as taught by Rolston et al. for the purpose of employing rapid ring protection switching within ring architecture that provides synchronous clocking.

Response to Arguments

3. Applicant's arguments filed on November 25, 2008 have been fully considered but they are not persuasive.

Applicant argues, *page 15 Paragraph 1 Lines 2-7 and page 16 Lines 8-13 "However, the primary reference of ROLSTON et al. does not use virtual circuits but rather uses multiple hard-wired channels. There is thus no reason to utilize virtual circuits in the technology of ROLSTON et al. Applying the technology of CEDRONE et al. thus changes the principle of operation of ROLSTON et al.*" , with respect to claim 1.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner respectfully disagrees since Cedrone et al. teach a system (Fig.1 @ 10) for "… employing the inventive rapid ring protection switching sets up corresponding virtual circuits over both the selected ring and the non-selected ring."

(Column 3 Lines 36-38) For example, Cetrone et al. teach in Fig.1 "… a system 10 that may be part of an ATM network includes a plurality of nodes 12 that are interconnected by a primary ring 14 and a secondary ring 16." (Column 5 Lines 37-40), such as those in Rolston. Also, Cedrone et al. teach that "Intermediate nodes manage traffic on a virtual path basis, … A decision to perform protection switching on the virtual path ring is made on the basis of the virtual paths, ..." (Column 1 Lines 55-64, Column 4 Lines 12-25).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ virtual paths to propagate data (a synchronous clock signal) in a ring architecture, a function to apply path degradation/failure detection and a function to apply ring protection (by selecting a secondary ring over a primary ring that is down (e.g. broken connection) in order to prevent any loss of data) as taught by Cedrone et al. within the ring architecture as taught by Rolston et al. for the purpose of employing rapid ring protection switching within ring architecture that provides synchronous clocking.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or early communications from the Examiner should be directed to Salvador E. Rivas whose telephone number is (571) 270-1784. The examiner can normally be reached on Monday-Friday from 7:30AM to 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Gregory B. Sefcheck can be reached on (571) 272- 3098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Salvador E. Rivas
S.E.R./ser

February 4, 2009

/Gregory B Sefcheck/

Primary Examiner, Art Unit 2419

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